Elastic Parallel Architectures

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Abstract

Multicore processors are more power-area-effective and more reliable than single-core processors. Because of that, they have become mainstream in all market segments, from high-end servers to desktop and mobile PCs, and industry's roadmap is heading towards an increasing degree of threading in all segments. However, single-thread performance still matters a lot, and will continue to be a very important differentiating factor of future highly-threaded processors. Some workloads are tough to parallelize, and Amdahl's law points out the importance of improving performance in all sections of a given application, including parts that have little thread-level parallelism.

Given the general-purpose nature of processors, they are expected to provide good performance for all types of workloads, despite of their very different characteristics in terms of parallelism. Many users nowadays are willing to have processors with more thread-level capabilities, but at the same time, the majority of them are also willing to have high performance for lightly threaded applications.

The ideal solution is to have a processor where resources can dynamically be devoted to exploit either thread-level or instruction-level parallelism, trying to find the best trade-off between both of them depending on the particular code that is being running. This approach is what we call an *Elastic Parallel Architecture*.

How to build an effective elastic parallel architecture is an open research question. This talk will discuss the benefits of this type of architecture, and will describe several approaches that are being investigated for implementing it, highlighting the main strengths and weaknesses of each of them.

Bio

Antonio González received his M.S. and Ph.D. degrees from the Universitat Politècnica de Catalunya (UPC), in Barcelona, Spain. He is the founding director of the Intel Barcelona Research Center, started in 2002, whose research focuses on new microarchitecture paradigms and code generation techniques for future microprocessors. Prior to this, he joined the faculty of the Computer Architecture Department of UPC in 1986, and became a Full Professor in 2002. He currently holds a part-time Professor position at this department.

Antonio González has published over 250 papers, has given over 80 invited talks, has filed over 40 patents and has advised 15 PhD theses in the areas of computer architecture and compilers. He has been an Associate Editor of the IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Systems, ACM Transactions on Architecture and Code Optimization, and Journal of Embedded Computing. He has served on over 100 program committees for international symposia in the field of computer architecture, including ISCA, MICRO, ASPLOS, HPCA, PACT, ICS, ISPASS, CASES and IPDPS. He has been program chair for ICS 2003,

ISPASS 2003, MICRO 2004 and HPCA 2008, and general chair for MICRO 2008, among other symposia.